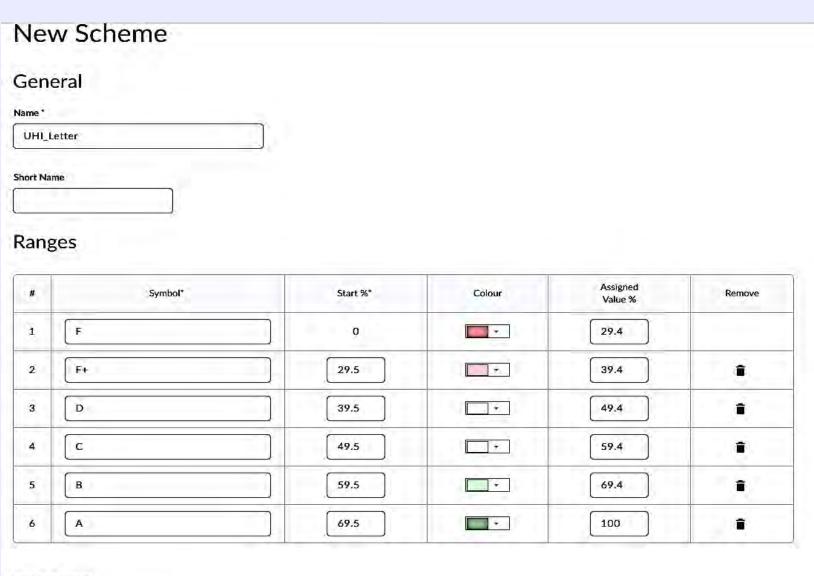# Mentoring Circle Coffee Meetings

Formative and Summative Coursework and Assessment in Brightspace

Elizabeth McFarlane, Tutor, Argyll College UHI

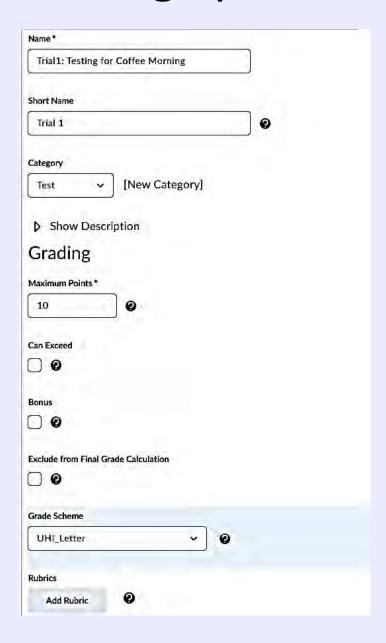Lois Gray, Academic Lead Developer, UHI

Setting up a Grading Scheme: Letter

New Scheme

General

Name *

UHI_Letter

Short Name

Ranges

#	Symbol*	Start %*	Colour	Assigned Value %	Remove
1	F	0		29.4	
2	F+	29.5		39.4	🗑
3	D	39.5		49.4	🗑
4	C	49.5		59.4	🗑
5	B	59.5		69.4	🗑
6	A	69.5		100	🗑

Number of Ranges

1   Add Ranges

Setting up a Grade Item and a Quiz

Name *

Trial1: Testing for Coffee Morning

Short Name

Trial 1 ❷

Category

Test ⌄ [New Category]

▷ Show Description

Grading

Maximum Points *

10 ❷

Can Exceed

☐ ❷

Bonus

☐ ❷

Exclude from Final Grade Calculation

☐ ❷

Grade Scheme

UHI_Letter ⌄ ❷

Rubrics

Add Rubric ❷

Question Library

New ⌄   Import ⌄

uestions

Section

True or False Question (T/F)

Multiple Choice Question (MC)

Multi-Select Question (M-S)

Written Response Question (WR)

Short Answer Question (SA)

Multi-Short Answer Question (MSA)

Fill in the Blanks Question (FIB)

Matching Question (MAT)

Ordering Question (ORD)

Arithmetic Question (2+2)

Significant Figures (x10)
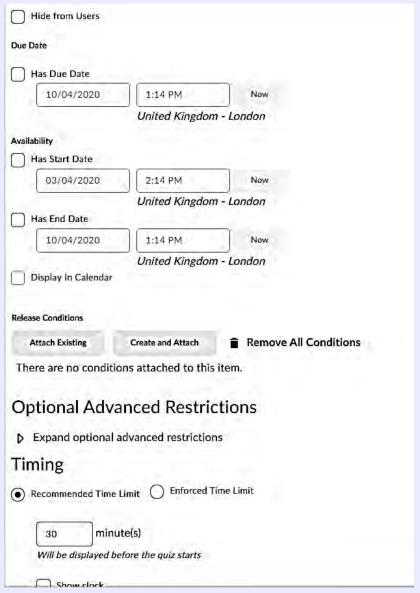
Likert Question (LIK)

Setting up Quiz Properties
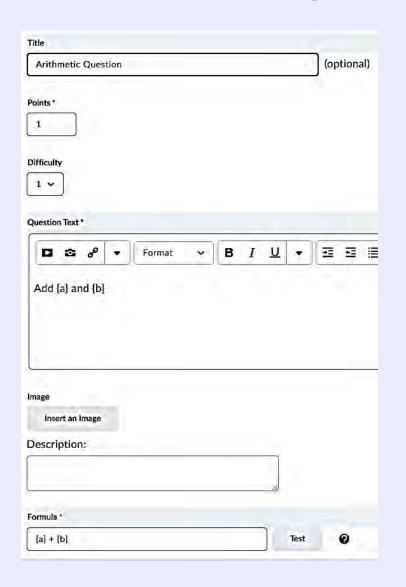
General

Name *

Sections 1 and 2: Analogue Integrated Circuits Self Assessment C

Category

no category ∨   [add category] ⊙

Quiz Questions

Questions per page: [   ]   **Apply**   ⊙

Paging: ☐ Prevent moving backwards through pages ⊙

☐ Shuffle questions at the quiz level
Also shuffles sections at the quiz level. Does not cascade to sub-sections.

Add/Edit Questions   **Edit Values**

Page	Name	Type	Points	Diff	Bonus	Mandatory
1	Q1. Current Mirror	2+2	1		3	
1	Q2. Current Mirror 2	2+2	1		3	
1	Q3. Current Mirror 3	M-S	1		3	
1	Q4. What kind of circuit is this?	MC	1		1	
1	Q5. Amplifier 2	2+2	1		1	
1	Q6. Amplifier 3	2+2	1		3	

Setting up Quiz Restrictions and Assessment

Hide from Users

Due Date

Has Due Date

| 10/04/2020 | 1:14 PM | Now |

United Kingdom - London

Availability

Has Start Date

| 03/04/2020 | 2:14 PM | Now |

United Kingdom - London

Has End Date

| 10/04/2020 | 1:14 PM | Now |

United Kingdom - London

Display In Calendar

Release Conditions

| Attach Existing | Create and Attach | 🗑 Remove All Conditions |

There are no conditions attached to this item.

Optional Advanced Restrictions

▷ Expand optional advanced restrictions

Timing

◉ Recommended Time Limit   ◯ Enforced Time Limit

| 30 | minute(s) |

Will be displayed before the quiz starts

Show clock

Assessment

Automatic Grade

Allow attempt to be set as graded immediately upon completion ❷

Grade Item

| Trial1: Testing for Coffee Morning ⌄ | [add grade item] ❷

Auto Export to Grades

Allow automatic export to grades ❷

Student View Preview

2 / 2 - A ⌄

ePortfolio Artefacts

Allow users to add the result of this quiz to their ePortfolio ❷

Attempts

Attempts Allowed ❷

| Unlimited ⌄ | Apply

Optional Advanced Attempt Conditions will appear if a number of attempts from 2 to 10 is applied.

Overall Grade Calculation

| Highest Attempt ⌄ |

Writing Arithmetic Questions

Title

Arithmetic Question   (optional)

Points *

1

Difficulty

1 ▾

Question Text *

| ▶ | ☘ | 🔗 | ▾ | | Format | ▾ | | **B** | *I* | U̲ | ▾ | | ⊞ | ⊟ | ☰ |

Add {a} and {b}

Image

Insert an Image

Description:

Formula *

[a] + [b]   Test   ❓

---

3 ▾   ☐ enforce precision   ▾

Tolerance

⦿ units +/- 0

◯ percent +/-

Units

[   ]   Worth: 0 ▾ % of Points

Evaluation Options:

⦿ Case Insensitive

◯ Case Sensitive

◯ Regular Expression

Variables

➕ **Add Variable** 1

#	Name	Min	Max	Decimal Places	Step	Remove
1	a	1	5	1 ▾	0.5	🗑
2	b	10	20	2 ▾	0.01	🗑

▷ Expand question hint

▾ Collapse question feedback

Question Feedback

Example Quiz

Sections 1 and 2: Analogue Integrated Circuits Self Assessment Questions (SAQs) - Preview

Exit Preview

Page 1:

1 --	2 --	3 --
4 --	5 --	6 --
7 --	8 --	9 --
10 --	11 --	12 --
13 --	14 --	

If the circuit in Q1 is changed so that the input side has two transistors as shown, what will be Iout3?

Your Answer:

Answer   units

Question 3 (1 point)

With the current mirror circuit, how can transistor mismatch be minimised? Select all correct answers.

- ☐ By using higher gain transistors
- ☐ By adding emitter resistors to all transistors
- ☐ By using lower gain transistors
- ☐ By making the microelectronic transistors the same size in the IC
- ☐ By putting the microelectronic transistors close together in the IC
- ☐ By buying the transistors from the same manufacturer

7

Creating Assignments & Editing Properties

Submission, Completion and Categorization

Assignment Type

- ● Individual assignment ❷
- ○ Group assignment ❷

  Group Category [-- No Group Categories Exist -- ˅]

Submission type

[File submission ˅]

Files Allowed Per Submission

- ● Unlimited
- ○ One file

Submissions

- ● All submissions are kept
- ○ Only the most recent submission is kept
- ○ Only one submission allowed

Notification Email

[   ] ❷

Category

[No Category ˅] [New Category]

Evaluation and Feedback

Score Out Of

[2] ❷

Evaluation and Feedback

Score Out Of

[2] ❷

Grade Item

[Coffee Morning Trial ˅] [New Grade Item]

Student View Preview

2 / 2 - 100 % ˅

Rubrics

[Add Rubric]

▦ Short Definition Rubric ✎ ✕

[Create Rubric in New Window]

Default Scoring Rubric

[Short Definition Rubric ˅] ❷

ePortfolio Artefacts

- ☑ Allow users to add this folder to their ePortfolio ❷

Anonymous Marking

- ☐ Hide student names during assessment

Annotation Tools

- ☑ Make annotation tools available for assessment

8

Using Rubrics

Criteria	Meets Expectations	Approaches Expectations	Doesn't Meet Expectations	
Focus (4 marks)	4 points Good reasoning and understanding of the topic are demonstrated	2.67 points Some reasoning and understanding of the topic is demonstrated	1.33 points Reasoning and understanding of the topic are not demonstrated	/ 4
Support (3 marks)	3 points Sufficient, appropriate evidence is included	2 points Some evidence is included but it may be insufficient or inappropriate	1 point Evidence is generally or largely absent	/ 3
Language (3 marks)	3 points The response has a formal style and has no errors which interfere with meaning	2 points The response attempts a formal style but contains some errors which interfere with meaning	1 point The response does not establish a formal style and contains several errors which interfere with meaning.	/ 3

Total	/ 10

Overall Score

Grade A 7 points minimum Distinction	Grade B 6 points minimum Very Good	Grade C 5 points minimum Good	Grade D 4 points minimum Pass	Grade F 0 points minimum Fail

Using Turnitin

Marking Assignments

	Assignment	New	Completed	Evaluated	Feedback Published	Due Date
☐	**No Category**					
☐	Coursework 1: VHDL Assignment ∨ 🔑 📇		14/25	14/25	14/25	03 November 2019 11:59 PM
☐	Coursework 2: Electronics Design Assignment ∨ 🔑 📇		13/25	13/25	13/25	06 December 2019 1:00 PM
☐	Resubmission Coursework 1 ∨ 📇	1	1/25	0/25	0/25	13 March 2020 1:30 PM
☐	Re-submission Coursework 2 ∨ 📇	1	1/25	0/25	0/25	13 March 2020 1:30 PM

20 per page ∨

Users   Submissions

View By: User ∨   Apply

🔍 Show Search Options

☁ Download   ✈ Email   📧 Mark as Read   ✉ Mark as Unread   🗑 Delete   🔑 Publish Feedback

☐	Last Name ▲ , First Name		Turnitin® Similarity	Turnitin® GradeMark®	Submission Date	Delete
☐					Published: 13 November 2019 2:14 PM	
	🏴 💻 VHDL Coursework 18003243.docx (2.38 MB)		21 % ▮	No Score ✎ ⇅	01 November 2019 2:38 AM	🗑
☐					Published: 13 November 2019 2:14 PM Feedback Read: 13 November 2019 2:36 PM	
	🏴 💻 Electronics 3 Coursework 1 Report..docx (22.64 MB) Electronics 3 Coursework number 1 Report from Liam Elder.		7 % ▮	No Score ✎ ⇅	27 October 2019 4:11 PM	🗑
☐	GUNN, CRAIG				Published: 24 November 2019 3:53 PM	
	🏴 💻 E3 Coursework A.docx (207.58 KB)		78 % ▮	No Score ✎ ⇅	11 November 2019 6:29 PM 🔧 7 days late	🗑

Marking Assignments