



Mentoring Circle Coffee Meetings



Formative and Summative
Coursework and Assessment
in Brightspace

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Setting up a Grading Scheme: Letter

New Scheme

General

Name*

UHI_Letter

Short Name

Ranges

#	Symbol*	Start %*	Colour	Assigned Value %	Remove
1	F	0		29.4	
2	F+	29.5		39.4	
3	D	39.5		49.4	
4	C	49.5		59.4	
5	B	59.5		69.4	
6	A	69.5		100	

Number of Ranges

1

Add Ranges

Setting up a Grade Item and a Quiz

Name*
Trial1: Testing for Coffee Morning

Short Name
Trial 1

Category
Test [New Category]

Show Description

Grading

Maximum Points*
10

Can Exceed

Bonus

Exclude from Final Grade Calculation

Grade Scheme
UHI_Letter

Rubrics
Add Rubric

Question Library

New Import

Section
True or False Question (T/F)
Multiple Choice Question (MC)
Multi-Select Question (M-S)
Written Response Question (WR)
Short Answer Question (SA)
Multi-Short Answer Question (MSA)
Fill in the Blanks Question (FIB)
Matching Question (MAT)
Ordering Question (ORD)
Arithmetic Question (2+2)
Significant Figures (x10)
Likert Question (LIK)

Setting up Quiz Properties

General

Name *

Sections 1 and 2: Analogue Integrated Circuits Self Assessment C

Category

no category ▾

[add category] ⓘ

Quiz Questions

Questions per page:

Apply



Paging: Prevent moving backwards through pages ⓘ

Shuffle questions at the quiz level
Also shuffles sections at the quiz level. Does not cascade to sub-sections.

Add/Edit Questions

Edit Values

Page Name	Type	Points	Diff	Bonus	Mandatory
1 Q1. Current Mirror	2+2	1	3		
1 Q2. Current Mirror 2	2+2	1	3		
1 Q3. Current Mirror 3	M-S	1	3		
1 Q4. What kind of circuit is this?	MC	1	1		
1 Q5. Amplifier 2	2+2	1	1		
1 Q6. Amplifier 3	2+2	1	3		

Setting up Quiz Restrictions and Assessment

Hide from Users

Due Date

Has Due Date

10/04/2020 1:14 PM Now
United Kingdom - London

Availability

Has Start Date

03/04/2020 2:14 PM Now
United Kingdom - London

Has End Date

10/04/2020 1:14 PM Now
United Kingdom - London

Display in Calendar

Release Conditions

Attach Existing Create and Attach Remove All Conditions

There are no conditions attached to this item.

Optional Advanced Restrictions

Expand optional advanced restrictions

Timing

Recommended Time Limit Enforced Time Limit

30 minute(s)
Will be displayed before the quiz starts

Show clock

Assessment

Automatic Grade

Allow attempt to be set as graded immediately upon completion

Grade Item

Trial1: Testing for Coffee Morning [add grade item]

Auto Export to Grades

Allow automatic export to grades

Student View Preview

2 / 2 - A

ePortfolio Artefacts

Allow users to add the result of this quiz to their ePortfolio

Attempts

Attempts Allowed

Unlimited Apply

Optional Advanced Attempt Conditions will appear if a number of attempts from 2 to 10 is applied.

Overall Grade Calculation

Highest Attempt

Writing Arithmetic Questions

Title
Arithmetic Question (optional)

Points *
1

Difficulty
1



Question Text *

Add {a} and {b}

Image
Insert an Image

Description:

Formula *
 Test 



3 enforce precision

Tolerance
 units +/- 0
 percent +/-

Units
 Worth: 0 % of Points

Evaluation Options:
 Case Insensitive
 Case Sensitive
 Regular Expression

Variables
+ Add Variable

#	Name	Min	Max	Decimal Places	Step	Remove
1	<input type="text" value="a"/>	<input type="text" value="1"/>	<input type="text" value="5"/>	<input type="text" value="1"/>	<input type="text" value="0.5"/>	
2	<input type="text" value="b"/>	<input type="text" value="10"/>	<input type="text" value="20"/>	<input type="text" value="2"/>	<input type="text" value="0.01"/>	

Expand question hint
 Collapse question feedback

Question Feedback

Example Quiz

Sections 1 and 2: Analogue Integrated Circuits Self Assessment Questions (SAQs) - Preview

Est. Length: 0:30:00

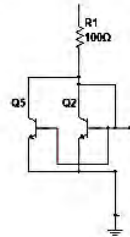
LOIS GRAY: Attempt 1

Exit Preview

Page 1:

1 --	2 --	3 --
4 --	5 --	6 --
7 --	8 --	9 --
10 --	11 --	12 --
13 --	14 --	

If the circuit in Q1 is changed so that the input side has two transistors as shown, what will be I_{out3} ?



Your Answer:

<input type="text"/>	<input type="text"/>
Answer	units

Question 3 (1 point)



With the current mirror circuit, how can transistor mismatch be minimised? Select all correct answers.


- By using higher gain transistors
- By adding emitter resistors to all transistors
- By using lower gain transistors
- By making the microelectronic transistors the same size in the IC
- By putting the microelectronic transistors close together in the IC
- By buying the transistors from the same manufacturer

Creating Assignments & Editing Properties


Submission, Completion and Categorization

Assignment Type

- Individual assignment 
- Group assignment 

Group Category -- No Group Categories Exist -- 

Submission type

File submission 

Files Allowed Per Submission

- Unlimited
- One file

Submissions

- All submissions are kept
- Only the most recent submission is kept
- Only one submission allowed

Notification Email




Category

No Category  [New Category]


Evaluation and Feedback

Score Out Of

2 

Evaluation and Feedback

Score Out Of

2 

Grade Item

Coffee Morning Trial  [\[New Grade Item\]](#)

Student View Preview

2 / 2 - 100 % 

Rubrics

[Add Rubric](#)


 [Short Definition Rubric](#)  

[\[Create Rubric in New Window\]](#)

Default Scoring Rubric

Short Definition Rubric  

ePortfolio Artefacts

Allow users to add this folder to their ePortfolio 

Anonymous Marking

Hide student names during assessment

Annotation Tools

Make annotation tools available for assessment

Using Rubrics

Criteria	Meets Expectations	Approaches Expectations	Doesn't Meet Expectations	
Focus (4 marks)	4 points Good reasoning and understanding of the topic are demonstrated	2.67 points Some reasoning and understanding of the topic is demonstrated	1.33 points Reasoning and understanding of the topic are not demonstrated	/ 4
Support (3 marks)	3 points Sufficient, appropriate evidence is included	2 points Some evidence is included but it may be insufficient or inappropriate	1 point Evidence is generally or largely absent	/ 3
Language (3 marks)	3 points The response has a formal style and has no errors which interfere with meaning	2 points The response attempts a formal style but contains some errors which interfere with meaning	1 point The response does not establish a formal style and contains several errors which interfere with meaning.	/ 3

Total	/ 10
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Overall Score

Grade A
7 points minimum
Distinction

Grade B
6 points minimum
Very Good

Grade C
5 points minimum
Good

Grade D
4 points minimum
Pass

Grade F
0 points minimum
Fail

Using Turnitin

Edit Assignment - Coffee Morning Trial

Properties Restrictions Objectives **Turnitin®**

Turnitin® Integration

GradeMark® ⓘ

Evaluation

- Enable GradeMark® for this folder
If you would like similarity scores to be generated, ensure you also enable Originality Check® below

Transfer

- Automatically sync grades as Draft in Brightspace ⓘ
 Manually sync grades as Draft in Brightspace

Originality Check® ⓘ

- Enable Originality Check® for this folder

Display

- Allow learners to see Turnitin® similarity scores in their submission folder

Frequency

- Automatic originality checking on all submissions
 Identify individual submissions for originality checking


More Options in Turnitin®

Submit File

AUTHOR	TITLE	SIMILARITY	GRADE
	Modelling of Open Loop Control System	0%	7
	Modelling of open loop control system	0%	8
	Modelling of Open Loop Control System	0%	5
	Modelling of Open Loop Control System	0%	10
	CW1	2%	8
	Modelling of hydraulic process control system	2%	7
	Coursework 1	2%	11
	Modelling of Open Loop Control System	3%	11
	Coursework 1	4%	8
	Coursework 1	5%	11
	Control Course Work 1	6%	10
	Modelling of Open Loop Control System	7%	8
	Modelling of Open Loop Control System	9%	11
	Coursework 1	11%	7
	Modelling of an Open Loop Control System	25%	9















Marking Assignments

<input type="checkbox"/>	Assignment	New	Completed	Evaluated	Feedback Published	Due Date
	No Category					
<input type="checkbox"/>	Coursework 1: VHDL Assignment   		14/25	14/25	14/25	03 November 2019 11:59 PM
<input type="checkbox"/>	Coursework 2: Electronics Design Assignment   		13/25	13/25	13/25	06 December 2019 1:00 PM
<input type="checkbox"/>	Resubmission Coursework 1  	1	1/25	0/25	0/25	13 March 2020 1:30 PM
<input type="checkbox"/>	Re-submission Coursework 2  	1	1/25	0/25	0/25	13 March 2020 1:30 PM

20 per page 

Users | Submissions

View By:

<input type="checkbox"/>	Last Name  , First Name	Turnitin® Similarity	Turnitin® GradeMark®	Submission Date	Delete
<input type="checkbox"/>				Published: 13 November 2019 2:14 PM	
<input type="checkbox"/>	 VHDL Coursework 18909243.docx (2.38 MB)	<div style="width: 21%;"><div style="background-color: green;">21 %</div></div>	No Score  	01 November 2019 2:38 AM	
<input type="checkbox"/>	 Electronics 3 Coursework 1 Report.docx (22.64 MB) Electronics 3 Coursework number 1 Report from Liam Elder.	<div style="width: 7%;"><div style="background-color: green;">7 %</div></div>	No Score  	27 October 2019 4:11 PM Published: 13 November 2019 2:14 PM Feedback Read: 13 November 2019 2:36 PM	
<input type="checkbox"/>	GUNN, CRAIG			Published: 24 November 2019 3:53 PM	
<input type="checkbox"/>	 E3 Coursework A.docx (207.58 KB)	<div style="width: 78%;"><div style="background-color: red;">78 %</div></div>	No Score  	11 November 2019 6:29 PM  7 days late	

Marking Assignments

The screenshot displays a Turnitin assignment marking interface. At the top left, there is a navigation link: [Back to User Submissions](#). The document title is `/HDL Coursework` (.docx) (2.38 MB), submitted by an unnamed user on 01 November 2019 at 2:38 AM. A "Launch Turnitin" button is visible in the top right.

The main area shows a document preview. The document title is "VHDL Coursework Tasks 1-7". The first task is titled "Task 1: Half Adder". The text of the task reads: "Using the 'SOLIVER' software, a new VHDL project is started and the half adder code is implemented to the specified device, named 'spMACH4000 LC41282E'. Names of inputs and outputs, libraries, and defining entities and architectures are put together within the software text editor, enabling the user to determine the function or mode of parts of the device." Below the text is a screenshot of a software interface showing code and a terminal window.

On the right side, the "Rubrics" panel shows the assignment name "Coursework 1: VHDL Tasks" and a "Level achieved: A". The "Score" section shows a score of 25 / 28, with a "Grade Item: Coursework 1" label. Below this is a "Student View Preview" showing "25 / 28 = 89.29 %". The "Feedback" section includes a toolbar with icons for adding files, recording audio, and recording video. The feedback text reads: "A well written report with explicit task introductions, well labelled supporting diagrams, and code comments which indicate good".